

MOS INTEGRATED CIRCUIT μPD44164084, 44164184, 44164364

18M-BIT DDRII SRAM 4-WORD BURST OPERATION

Description

The μ PD44164084 is a 2,097,152-word by 8-bit, the μ PD44164184 is a 1,048,576-word by 18-bit and the μ PD44164364 is a 524,288-word by 36-bit synchronous double data rate static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell.

The μ PD44164084, μ PD44164184 and μ PD44164364 integrates unique synchronous peripheral circuitry and a burst counter. All input registers controlled by an input clock pair (K and /K) are latched on the positive edge of K and /K.

These products are suitable for application which require synchronous operation, high speed, low voltage, high density and wide bit configuration.

These products are packaged in 165-pin PLASTIC BGA.

Features

- 1.8 ± 0.1 V power supply and HSTL I/O
- DLL circuitry for wide output data valid window and future frequency scaling
- Pipelined double data rate operation
- Common data input/output bus
- Four-tick burst for reduced address frequency
- Two input clocks (K and /K) for precise DDR timing at clock rising edges only
- Two output clocks (C and /C) for precise flight time and clock skew matching-clock and data delivered together to receiving device
- Internally self-timed write control
- Clock-stop capability with µs restart
- User programmable impedance output
- Fast clock cycle time: 4.0 ns (250 MHz), 5.0 ns (200 MHz), 6.0 ns (167 MHz)
- Simple control logic for easy depth expansion
- JTAG boundary scan

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★ Ordering Information

Part number	Cycle	Clock	Organization	Core Supply	I/O	Package
	Time	Frequency	(word x bit)	Voltage	Interface	
	ns	MHz		V		
μPD44164084F5-E40-EQ1	4.0	250	2 M x 8-bit	1.8 ± 0.1	HSTL	165-pin PLASTIC
μPD44164084F5-E50-EQ1	5.0	200				BGA (13 x 15)
μPD44164084F5-E60-EQ1	6.0	167				
μPD44164184F5-E40-EQ1	4.0	250	1 M x 18-bit			
μPD44164184F5-E50-EQ1	5.0	200				
μPD44164184F5-E60-EQ1	6.0	167				
μPD44164364F5-E50-EQ1	5.0	200	512 K x 36-bit			
μPD44164364F5-E60-EQ1	6.0	167				



Pin Configurations

/xxx indicates active low signal.

165-pin PLASTIC BGA (13 x 15) (Top View) [μPD44164084F5-EQ1]

	1	2	3	4	5	6	7	8	9	10	11
Α	/CQ	Vss	A	R, /W	/NW1	/K	NC	/LD	Α	Vss	CQ
В	NC	NC	NC	Α	NC	К	/NW0	Α	NC	NC	DQ3
С	NC	NC	NC	Vss	Α	NC	Α	Vss	NC	NC	NC
D	NC	NC	NC	Vss	Vss	Vss	Vss	Vss	NC	NC	NC
Ε	NC	NC	DQ4	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	DQ2
F	NC	NC	NC	VDDQ	V DD	Vss	V DD	VDDQ	NC	NC	NC
G	NC	NC	DQ5	VDDQ	V DD	Vss	V DD	VDDQ	NC	NC	NC
н	/DLL	VREF	VDDQ	VDDQ	V DD	Vss	V DD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	NC	VDDQ	V DD	Vss	V DD	VDDQ	NC	DQ1	NC
κ	NC	NC	NC	VDDQ	V DD	Vss	V DD	VDDQ	NC	NC	NC
L	NC	DQ6	NC	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	DQ0
M	NC	NC	NC	Vss	Vss	Vss	Vss	Vss	NC	NC	NC
N	NC	NC	NC	Vss	Α	Α	Α	Vss	NC	NC	NC
Р	NC	NC	DQ7	Α	Α	С	Α	Α	NC	NC	NC
R	TDO	тск	Α	Α	Α	/C	Α	Α	Α	тмѕ	TDI

: Address inputs : IEEE 1149.1 Test input **TMS** DQ0 to DQ7 : Data inputs / outputs TDI : IEEE 1149.1 Test input /LD : Synchronous load TCK : IEEE 1149.1 Clock input R, /W : Read Write input TDO : IEEE 1149.1 Test output /NW0, /NW1 : Nibble Write data select V_{REF} : HSTL input reference input

K, /K : Power Supply : Input clock V_{DD} C, /C : Output clock $V_{DD}Q$: Power Supply CQ, /CQ : Echo clock Vss : Ground ZQ : Output impedance matching NC : No connection

/DLL : DLL disable

Remark Refer to Package Drawing for the index mark.

165-pin PLASTIC BGA (13 x 15) (Top View) [*µ*PD44164184F5-EQ1]

	1	2	3	4	5	6	7	8	9	10	11
Α	/CQ	V ss	A	R, /W	/BW1	/K	NC	/LD	Α	Vss	CQ
В	NC	DQ9	NC	Α	NC	K	/BW0	A	NC	NC	DQ8
С	NC	NC	NC	V ss	Α	Α0	A 1	Vss	NC	DQ7	NC
D	NC	NC	DQ10	Vss	Vss	Vss	Vss	Vss	NC	NC	NC
Ε	NC	NC	DQ11	V _{DD} Q	Vss	Vss	Vss	VDDQ	NC	NC	DQ6
F	NC	DQ12	NC	V _{DD} Q	V DD	Vss	V DD	VDDQ	NC	NC	DQ5
G	NC	NC	DQ13	V _{DD} Q	V DD	Vss	V DD	VDDQ	NC	NC	NC
н	/DLL	VREF	VDDQ	VDDQ	V DD	Vss	V DD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	NC	V _{DD} Q	V DD	Vss	V DD	VDDQ	NC	DQ4	NC
K	NC	NC	DQ14	V _{DD} Q	V DD	Vss	V DD	VDDQ	NC	NC	DQ3
L	NC	DQ15	NC	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	DQ2
М	NC	NC	NC	Vss	Vss	Vss	Vss	Vss	NC	DQ1	NC
N	NC	NC	DQ16	Vss	Α	Α	Α	Vss	NC	NC	NC
Р	NC	NC	DQ17	Α	Α	С	Α	Α	NC	NC	DQ0
R	TDO	тск	Α	Α	Α	/C	Α	Α	Α	тмѕ	TDI

A0, A1, A : Address inputs **TMS** : IEEE 1149.1 Test input DQ0 to DQ17 : Data inputs / outputs TDI : IEEE 1149.1 Test input : Synchronous load /LD **TCK** : IEEE 1149.1 Clock input R, /W : IEEE 1149.1 Test output : Read Write input TDO /BW0, /BW1 : Byte Write data select V_{REF} : HSTL input reference input

K, /K : Input clock V_{DD} : Power Supply C, /C : Power Supply : Output clock $V_{DD}Q$ CQ, /CQ : Echo clock Vss : Ground ZQ : Output impedance matching NC : No connection

/DLL : DLL disable

Remark Refer to Package Drawing for the index mark.

165-pin PLASTIC BGA (13 x 15) (Top View) [*µ*PD44164364F5-EQ1]

	1	2	3	4	5	6	7	8	9	10	11
Α	/CQ	Vss	NC	R, /W	/BW2	/K	/BW1	/LD	A	Vss	cq
В	NC	DQ27	DQ18	Α	/BW3	K	/BW0	Α	NC	NC	DQ8
С	NC	NC	DQ28	Vss	Α	Α0	A 1	Vss	NC	DQ17	DQ7
D	NC	DQ29	DQ19	Vss	Vss	Vss	Vss	Vss	NC	NC	DQ16
E	NC	NC	DQ20	VDDQ	Vss	Vss	Vss	VDDQ	NC	DQ15	DQ6
F	NC	DQ30	DQ21	VDDQ	V DD	Vss	V DD	VDDQ	NC	NC	DQ5
G	NC	DQ31	DQ22	VDDQ	V DD	Vss	V DD	VDDQ	NC	NC	DQ14
н	/DLL	VREF	VDDQ	VDDQ	V DD	Vss	V DD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	DQ32	VDDQ	V DD	Vss	V DD	VDDQ	NC	DQ13	DQ4
ĸ	NC	NC	DQ23	VDDQ	V DD	Vss	V DD	VDDQ	NC	DQ12	DQ3
L	NC	DQ33	DQ24	VDDQ	Vss	Vss	Vss	VDDQ	NC	NC	DQ2
M	NC	NC	DQ34	Vss	Vss	Vss	Vss	Vss	NC	DQ11	DQ1
N	NC	DQ35	DQ25	Vss	Α	Α	Α	Vss	NC	NC	DQ10
Р	NC	NC	DQ26	Α	Α	С	Α	Α	NC	DQ9	DQ0
R	TDO	тск	Α	Α	Α	/C	Α	Α	Α	тмѕ	TDI

A0, A1, A : Address inputs **TMS** : IEEE 1149.1 Test input DQ0 to DQ35 : Data inputs / outputs TDI : IEEE 1149.1 Test input : Synchronous load /LD TCK : IEEE 1149.1 Clock input R, /W : IEEE 1149.1 Test output : Read Write input TDO /BW0 to /BW3 : Byte Write data select V_{REF} : HSTL input reference input

K, /K : Input clock V_{DD} : Power Supply C, /C : Power Supply : Output clock $V_{DD}Q$ CQ, /CQ Vss : Echo clock : Ground ZQ : Output impedance matching NC : No connection

/DLL : DLL disable

Remark Refer to Package Drawing for the index mark.

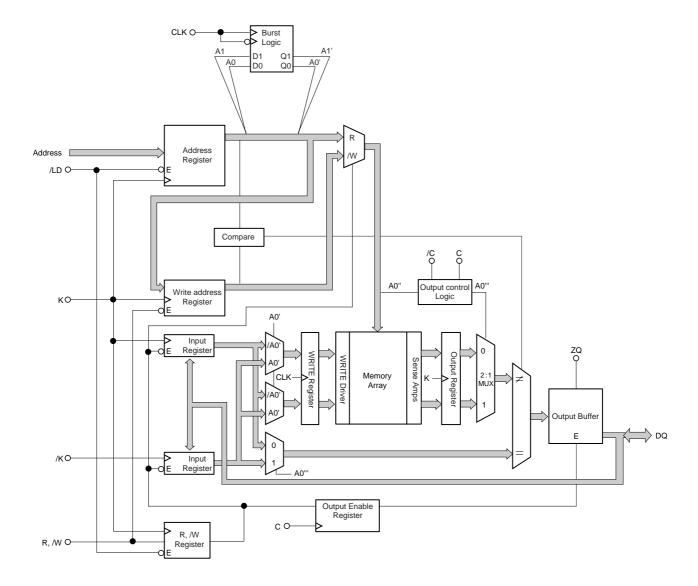


Pin Identification

Symbol	Description
A0	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the
A1	rising edge of K. Balls 3A, 10A, and 2A are reserved for the next higher-order address inputs on future devices.
Α	All transactions operate on a burst of four words (two clock periods of bus activity). A0 and A1 are used as the
	lowest two address bits for BURST READ and BURST WRITE operations permitting a random burst start
	address on x18 and x36 devices. These inputs are ignored when device is deselected or once BURST
	operation is in progress.
DQ0 to DQxx	Synchronous Data IOs: Input data must meet setup and hold times around the rising edges of K and /K. Output
	data is synchronized to the respective C and /C data clocks or to K and /K if C and /C are tied to HIGH.
	x8 device uses DQ0 to DQ7.
	x18 device uses DQ0 to DQ17.
	x36 device uses DQ0 to DQ35.
/LD	Synchronous Load: This input is brought LOW when a bus cycle sequence is to be defined. This definition
	includes address and read/write direction. All transactions operate on a burst of 4 data (two clock periods of bus
	activity).
R, /W	Synchronous Read/Write Input: When /LD is LOW, this input designates the access type (READ when R, /W is
	HIGH, WRITE when R, /W is LOW) for the loaded address. R, /W must meet the setup and hold times around
	the rising edge of K.
/BWx	Synchronous Byte Writes (Nibble Writes on x8): When LOW these inputs cause their respective byte or nibble
/NWx	to be registered and written during WRITE cycles. These signals must meet setup and hold times around the
	rising edges of K and /K for each of the two rising edges comprising the WRITE cycle. See Pin Configurations
	for signal to data relationships.
K, /K	Input Clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data
	on the rising edge of K and the rising edge of /K. /K is ideally 180 degrees out of phase with K. All synchronous
	inputs must meet setup and hold times around the clock rising edges.
C, /C	Output Clock: This clock pair provides a user controlled means of tuning device output data. The rising edge of
	/C is used as the output timing reference for first and third output data. The rising edge of C is used as the
	output reference for second and fourth output data. Ideally, /C is 180 degrees out of phase with C. C and /C
	may be tied HIGH to force the use of K and /K as the output reference clocks instead of having to provide C and
	/C clocks. If tied HIGH, C and /C must remain HIGH and not be toggled during device operation.
CQ, /CQ	Synchronous Echo Clock Outputs. The rising edges of these outputs are tightly matched to the synchronous
	data outputs and can be used as a data valid indication. These signals run freely and do not stop when Q
	tristates.
ZQ	Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus
	impedance. DQ and CQ output impedance are set to 0.2 x RQ, where RQ is a resistor from this bump to
	ground. This pin cannot be connected directly to GND or left unconnected. Also, in this product, there is no
	function to minimize the output impedance by connecting ZQ directly to VDQ.
/DLL	DLL Disable: When LOW, this input causes the DLL to be bypassed for stable low frequency operation.
TMS	IEEE 1149.1 Test Inputs: 1.8V I/O levels. These balls may be left Not Connected if the JTAG function is not
TDI	used in the circuit.
TCK	IEEE 1149.1 Clock Input: 1.8V I/O levels. This pin must be tied to Vss if the JTAG function is not used in the
	circuit.
TDO	IEEE 1149.1 Test Output: 1.8V I/O level.
VREF	HSTL Input Reference Voltage: Nominally V _{DD} Q/2. Provides a reference voltage for the input buffers.
VDD	Power Supply: 1.8V nominal. See DC Characteristics and Operating Conditions for range.
VDDQ	Power Supply: Isolated Output Buffer Supply. Nominally 1.5V. 1.8V is also permissible. See DC Characteristics
	and Operating Conditions for range.
Vss	Power Supply: Ground
NC	No Connect: These signals are internally connected and appear in the JTAG scan chain as the logic level
	applied to the ball sites. These signals may be connected to ground to improve package heat dissipation.



Block Diagram



Burst Sequence

Linear Burst Sequence Table

[μ PD44164184, μ PD44164364]

	A1, A0	A1, A0	A1, A0	A1, A0
External Address	0, 0	0, 1	1, 0	1, 1
1st Internal Burst Address	0, 1	1, 0	1, 1	0, 0
2nd Internal Burst Address	1, 0	1, 1	0, 0	0, 1
3rd Internal Burst Address	1, 1	0, 0	0, 1	1, 0

Truth Table

Operation	/LD	R, /W	CLK		DQ				
WRITE cycle	L	L	$L \rightarrow H$	Data in					
Load address, input write data on two					Input data	D(A1)	D(A2)	D(A3)	D(A4)
consecutive K and /K rising edge					Input clock	K(t+1) ↑	/K(t+1) ↑	K(t+2) ↑	/K(t+2) ↑
READ cycle	L	Н	$L\toH$	Data out					
Load address, read data on two					Output data	Q(A1)	Q(A2)	Q(A3)	Q(A4)
consecutive C and /C rising edge					Output clock	/C(t+1) ↑	C(t+2) ↑	/C(t+2) ↑	C(t+3) ↑
NOP (No operation)	Η	Х	$L \rightarrow H$	High-Z					
STANDBY(Clock stopped)	Χ	Х	Stopped	Previous	state				

Remarks 1. H: High level, L: Low level, \times : don't care, \uparrow : rising edge.

- 2. Data inputs are registered at K and /K rising edges. Data outputs are delivered at C and /C rising edges except if C and /C are HIGH then Data outputs are delivered at K and /K rising edges.
- All control inputs in the truth table must meet setup/hold times around the rising edge (LOW to HIGH) of K. All control inputs are registered during the rising edge of K.
- 4. This device contains circuitry that will ensure the outputs will be in high impedance during power-up.
- **5.** Refer to state diagram and timing diagrams for clarification.
- **6.** A1 refers to the address input during a WRITE or READ cycle. A2, A3 and A4 refer to the next internal burst address in accordance with the linear burst sequence.
- 7. It is recommended that K = /K = C = /C when clock is stopped. This is not essential but permits most rapid restart by overcoming transmission line charging symmetrically.



Byte Write Operation

[*µ*PD44164084]

Operation	K	/K	/NW0	/NW1
Write DQ0 to DQ7	$L \rightarrow H$	_	0	0
	_	$L \rightarrow H$	0	0
Write DQ0 to DQ3	$L \rightarrow H$	_	0	1
	_	$L \rightarrow H$	0	1
Write DQ4 to DQ7	$L \rightarrow H$	_	1	0
	_	$L \rightarrow H$	1	0
Write nothing	$L \rightarrow H$	_	1	1
	_	$L \rightarrow H$	1	1

Remark H: High level, L: Low level, \rightarrow : rising edge.

[*µ*PD44164184]

Operation	K	/K	/BW0	/BW1
Write DQ0 to DQ17	$L \rightarrow H$	-	0	0
	_	$L \rightarrow H$	0	0
Write DQ0 to DQ8	$L \rightarrow H$	_	0	1
	_	$L \rightarrow H$	0	1
Write DQ9 to DQ17	$L \rightarrow H$	_	1	0
	_	$L \rightarrow H$	1	0
Write nothing	$L \rightarrow H$	_	1	1
	_	$L \rightarrow H$	1	1

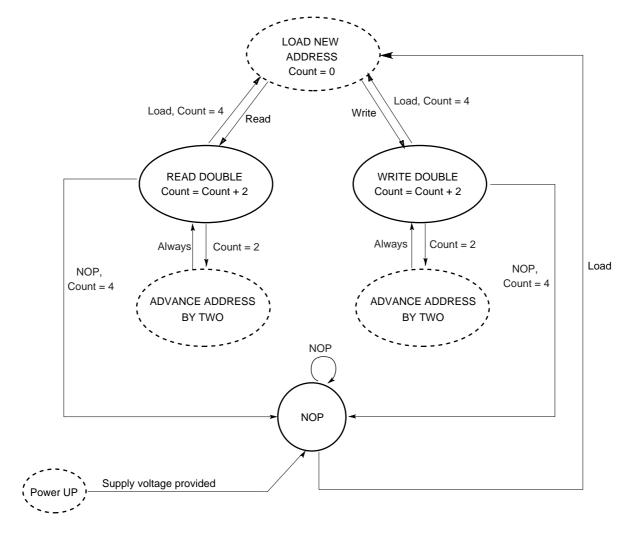
Remark H: High level, L: Low level, \rightarrow : rising edge.

[µPD44164364]

Operation	K	/K	/BW0	/BW1	/BW2	/BW3
Write DQ0 to DQ35	$L\toH$	-	0	0	0	0
	_	$L \rightarrow H$	0	0	0	0
Write DQ0 to DQ8	$L \rightarrow H$	_	0	1	1	1
	_	$L \rightarrow H$	0	1	1	1
Write DQ9 to DQ17	$L \rightarrow H$	_	1	0	1	1
	_	$L \rightarrow H$	1	0	1	1
Write DQ18 to DQ26	$L\toH$	_	1	1	0	1
	-	$L \rightarrow H$	1	1	0	1
Write DQ27 to DQ35	$L\toH$	_	1	1	1	0
	-	$L \rightarrow H$	1	1	1	0
Write nothing	$L\toH$	_	1	1	1	1
	_	$L \rightarrow H$	1	1	1	1

 $\textbf{Remark} \quad \text{H}: \text{High level, L}: \text{Low level,} \rightarrow : \text{rising edge}.$

Bus Cycle State Diagram



Remarks 1. A0 and A1 are internally advanced in accordance with the burst order table. Bus cycle is terminated after burst count = 4.

- 2. State transitions: L = (/LD = LOW); /L = (/LD = HIGH); R = (/R, W = HIGH); W = (/R, W = LOW).
- 3. State machine control timing sequence is controlled by K.



Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	VDD		-0.5		+2.9	V
Output supply voltage	VDDQ		-0.5		VDD	V
Input voltage	VIN		-0.5		VDD + 0.5 (2.9 V MAX.)	V
Input / Output voltage	VI/O		-0.5		VDDQ + 0.5 (2.9 V MAX.)	V
Operating ambient temperature	TA		0		70	°C
Storage temperature	Tstg		- 55		+125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	VDD		1.7		1.9	V	
Output supply voltage	VDDQ		1.4		VDD	V	1
High level input voltage	VIH (DC)		VREF + 0.1		V _{DD} Q + 0.3	V	1, 2
Low level input voltage	VIL (DC)		-0.3		VREF - 0.1	V	1, 2
Clock input voltage	VIN		-0.3		V _{DD} Q + 0.3	V	1, 2
Reference voltage	VREF		0.68		0.95	V	

Notes 1. During normal operation, VDDQ must not exceed VDD.

2. Power-up: $V_{IH} \le V_{DD}Q + 0.3 \text{ V}$ and $V_{DD} \le 1.7 \text{ V}$ and $V_{DD}Q \le 1.4 \text{ V}$ for $t \le 200 \text{ ms}$

Recommended AC Operating Conditions (TA = 0 to 70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
High level input voltage	VIH (AC)		VREF + 0.2		-	V	1
Low level input voltage	VIL (AC)		-		VREF - 0.2	٧	1

Note 1. Overshoot: $V_{IH (AC)} \le V_{DD} + 0.7 V$ for $t \le TKHKH/2$

Undershoot: $V_{IL\ (AC)} \ge -0.5\ V$ for $t \le TKHKH/2$

Control input signals may not have pulse widths less than TKHKL (MIN.) or operate at cycle rates less than TKHKH (MIN.).



DC Characteristics (T_A = 0 to 70° C, V_{DD} = $1.8 \pm 0.1 \text{ V}$)

	Parameter	Symbol	Test condition		MIN.	TYP.	MAX.		Unit	Note
							x8, x18	x36		
	Input leakage current	lu			-2	_	+,	2	μΑ	
	I/O leakage current	llo			-2	-	+	2	μΑ	
*	Operating supply current	IDD	$VIN \le VIL \text{ or } VIN \ge VIH,$	-E40			620	-	mA	
	(Read Write cycle)		I _{I/O} = 0 mA	-E50			540	620		
			Cycle = MAX.	-E60			470	570		
*	Standby supply current	ISB1	$VIN \le VIL \text{ or } VIN \ge VIH,$	-E40			320	-	mA	
	(NOP)		I _{I/O} = 0 mA	-E50			27	70		
			Cycle = MAX.	-E60			25	50		
	High level output voltage	VOH(Low)	IOH ≤ 0.1 mA	Iон ≤ 0.1 mA		-	VDI	DQ	V	3, 4
		Vон	Note1		VDDQ/2-0.12	_	VDDQ/2	2+0.12	V	3, 4
	Low level output voltage	VOL(Low)	IoL ≤ 0.1 mA		Vss	_	0.	2	V	3, 4
		Vol	Note2		VDDQ/2-0.12	_	VDDQ/2	2+0.12	V	3, 4

- **Notes 1.** Outputs are impedance-controlled. | IoH | = (VDDQ/2)/(RQ/5) for values of 175 $\Omega \le RQ \le 350 \ \Omega$.
 - **2.** Outputs are impedance-controlled. IoL = $(V_{DD}Q/2)/(RQ/5)$ for values of 175 $\Omega \le RQ \le 350 \ \Omega$.
 - 3. AC load current is higher than the shown DC values.
 - **4.** HSTL outputs meet JEDEC HSTL Class I and Class II standards.

Capacitance (TA = 25 °C, f = 1MHz)

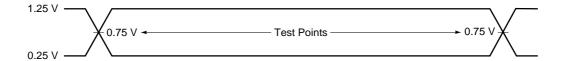
Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	Cin	VIN = 0 V		4	5	pF
Input / Output capacitance	Cı/o	VI/O = 0 V		6	7	pF
Clock Input capacitance	Cclk	Vclk = 0 V		5	6	pF

Remark These parameters are periodically sampled and not 100% tested.

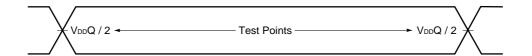
AC Characteristics (T_A = 0 to 70 °C, V_{DD} = 1.8 ± 0.1 V)

AC Test Conditions

Input waveform (Rise / Fall time ≤ 0.3 ns)

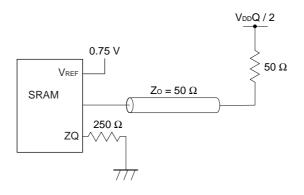


Output waveform



Output load condition

Figure 1. External load at test





Read and Write Cycle

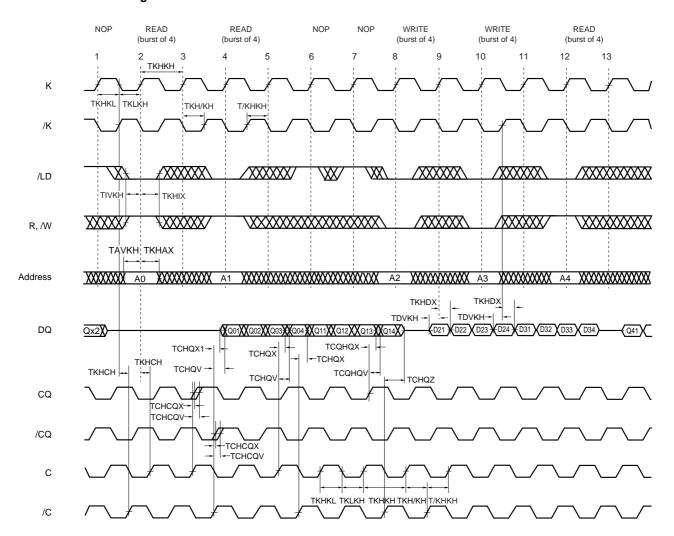
Param	eter	Symbol	-E4 (250)		-E:		-E(Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	1	
Clock			WIII V.	Wir U.	IVIII V.	Wir U.	Will V.	Wir U.		
Average Clock cycle	time (K /K C /C)	TKHKH	4.0	8.4	5.0	8.4	6.0	8.4	ns	1
Clock phase jitter (K,		TKC var	- 1.0	0.4	-	0.4	-	0.4	ns	2
Clock HIGH time (K,		TKHKL	1.6	-	2.0	-	2.4	-	ns	
Clock LOW time (K,	,	TKLKH	1.6	_	2.0	_	2.4	_	ns	
Clock to /clock (K→/		TKH /KH	1.8	_	2.2	_	2.7	_	ns	
Clock to /clock (/K→		T /KHKH	1.8	_	2.2	_	2.7	_	ns	
Clock to data clock	200 to 250 MHz	TKHCH	0	1.8	_	_	_	_	ns	
(K→C., /K→/C.)	167 to 200 MHz	•	0	2.3	0	2.3	_	_		
, , , , , , , , , , , , , , , , , , , ,	133 to 167 MHz	•	0	2.8	0	2.8	0	2.8		
	< 133 MHz		0	3.55	0	3.55	0	3.55		
DLL lock time (K, C)		TKC lock	1,024	_	1,024	_	1,024	_	Cycle	3
K static to DLL reset		TKC reset	30	_	30	_	30	_	ns	
		l l		I.	l .	l .				
Output Times		1								
C, /C HIGH to output	t valid	TCHQV	_	0.45	_	0.45	_	0.5	ns	
C, /C HIGH to output		TCHQX	-0.45	_	-0.45	_	-0.5	_	ns	
C, /C HIGH to echo		TCHCQV	_	0.45	_	0.45	_	0.5	ns	
C, /C HIGH to echo	clock hold	TCHCQX	-0.45	_	-0.45	_	-0.5	_	ns	
CQ, /CQ HIGH to ou	tput valid	TCQHQV	_	0.3	_	0.35	_	0.4	ns	4
CQ, /CQ HIGH to ou	tput hold	TCQHQX	-0.3	_	-0.35	_	-0.4	_	ns	4
C HIGH to output Hig	gh-Z	TCHQZ	_	0.45	_	0.45	_	0.5	ns	
C HIGH to output Lo	w-Z	TCHQX1	-0.45	-	-0.45	-	-0.5	-	ns	
		_								
Setup Times										
Address valid to K ris	sing edge	TAVKH	0.5	_	0.6	_	0.7	_	ns	5
Synchronous load in	put (/LD),	TIVKH	0.5	-	0.6	_	0.7	_	ns	5
read write input (R, /	W) valid to									
K rising edge										
Data inputs and write	e data select	TDVKH	0.35	-	0.4	_	0.5	_	ns	5
inputs (/BWx, /NWx)	valid to									
K, /K rising edge	K, /K rising edge									
		1								
Hold Times				1	1	1			_	
K rising edge to address hold		TKHAX	0.5	_	0.6	-	0.7	_	ns	5
K rising edge to		TKHIX	0.5	_	0.6	_	0.7	_	ns	5
synchronous load input (/LD),										
read write input (R, /										
K, /K rising edge to c		TKHDX	0.35	_	0.4	_	0.5	-	ns	5
write data select inpu	ıts (/BWx, /NWx)									
hold										

- **Notes 1.** The device will operate at clock frequencies slower than TKHKH(MAX.).
 - 2. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
 - 3. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention.
 - DLL lock time begins once V_{DD} and input clock are stable.
 - It is recommended that the device is kept inactive during these cycles.
 - **4.** Echo clock is very tightly controlled to data valid / data hold. By design, there is a \pm 0.1 ns variation from echo clock to data. The data sheet parameters reflect tester guardbands and test setup variations.
 - **5.** This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.

Remarks 1. This parameter is sampled.

- **2.** Test conditions as specified with the output loading as shown in AC Test Conditions unless otherwise noted.
- 3. Control input signals may not be operated with pulse widths less than TKHKL (MIN.).
- 4. If C, /C are tied HIGH, K, /K become the references for C, /C timing parameters.
- **5.** V_{DD}Q is 1.5 V DC.

Read and Write Timing



Remarks 1. Q01 refers to output from address A0.

Q02 refers to output from the next internal burst address following A0, etc.

- 2. Outputs are disable (high impedance) one clock cycle after a NOP.
- **3.** The second NOP cycle is not necessary for correct device operation; however, at high clock frequencies it may be required to prevent bus contention.



JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

Test Access Port (TAP) Pins

Pin name	Pin assignments	Description
TCK	2R	Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	10R	Test Mode Select. This is the command input for the TAP controller state machine.
TDI	11R	Test Data Input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.
TDO	1R	Test Data Output. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Remark The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held high for five rising edges of TCK. The TAP controller state is also reset on the SRAM POWER-UP.

JTAG DC Characteristics (T_A = 0 to 70°C, V_{DD} = 1.8 ± 0.1 V, unless otherwise noted)

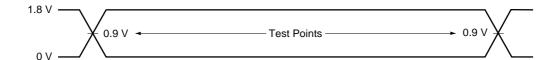
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
JTAG Input leakage current	lц	$0 \text{ V} \leq V_{IN} \leq V_{DD}$	-5.0	-	+5.0	μΑ	
JTAG I/O leakage current	ILO	$0 \text{ V} \leq V_{IN} \leq V_{DD}Q,$	-5.0	_	+5.0	μΑ	
		Outputs disabled					
JTAG input high voltage	ViH		1.3	-	V _{DD} + 0.3	٧	
JTAG input low voltage	VIL		-0.3	_	+0.5	٧	
JTAG output high voltage	Voh1	Ioнc = 100 μA	1.6	_	-	٧	
	VOH2	Іонт = 2 mA	1.4	_	-	٧	
JTAG output low voltage	V _{OL1}	IoLC = 100 μA	_	_	0.2	٧	
	VOL2	IOLT = 2 mA	_	_	0.4	٧	

Data Sheet M15822EJ7V1DS

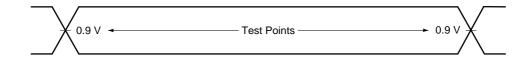
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JTAG AC Test Conditions

Input waveform (Rise / Fall time ≤ 1 ns)

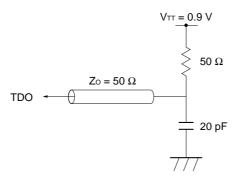


Output waveform



Output load

Figure 2. External load at test

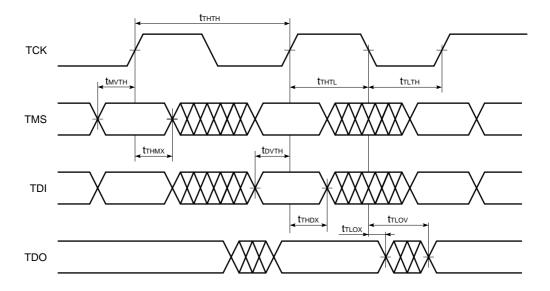




JTAG AC Characteristics (T_A = 0 to 70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Clock							
Clock cycle time	tтнтн		100	_	_	ns	
Clock frequency	f⊤⊧		_	_	10	MHz	
Clock high time	tтнт∟		40	_	_	ns	
Clock low time	tтьтн		40	-	_	ns	
Output time	7						
TCK low to TDO unknown	t TLOX		0	_	_	ns	
TCK low to TDO valid	t TLOV		_	-	20	ns	
TDI valid to TCK high	tоvтн		10	_	_	ns	
TCK high to TDI invalid	tтнох		10	-	_	ns	
Setup time	7						
TMS setup time	tмvтн		10	_	_	ns	
Capture setup time	tcs		10	-	-	ns	
Hold time	7						
TMS hold time	tтнмх		10	_	_	ns	
Capture hold time	tсн		10	_	_	ns	

JTAG Timing Diagram





Scan Register Definition (1)

Register name	Description
Instruction register	The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run-test/idle or the various data register state. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state.
Bypass register	The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.
ID register	The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state.
Boundary register	The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register. The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The second column is the name of the input or I/O at the bump and the third column is the bump number.

Scan Register Definition (2)

Register name	Bit size	Unit	
Instruction register	3	bit	
Bypass register	1	bit	
ID register	32	bit	
Boundary register	107	bit	

ID Register Definition

Part number	Organization	ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
μPD44164084	2M x 8	XXXX	0000 0000 0001 0101	0000010000	1
μPD44164184	1M x 18	XXXX	0000 0000 0001 0110	0000010000	1
μPD44164364	512K x 36	XXXX	0000 0000 0001 0111	00000010000	1



SCAN Exit Order

Bit	Sig	gnal na	me	Bump
no.	x8	x18	x36	ID
1		6R		
2		6P		
3		Α		6N
4		Α		7P
5		Α		7N
6		Α		7R
7		Α		8R
8		Α		8P
9		Α		9R
10	NC	DQ0	DQ0	11P
11	NC	NC	DQ9	10P
12	NC	NC	NC	10N
13	NC	NC	NC	9P
14	NC	DQ1	DQ11	10M
15	NC	NC	DQ10	11N
16	NC	NC	NC	9M
17	NC	NC	NC	9N
18	DQ0	DQ2	DQ2	11L
19	NC	NC	DQ1	11M
20	NC	NC	NC	9L
21	NC	NC	NC	10L
22	NC	DQ3	DQ3	11K
23	NC	NC	DQ12	10K
24	NC	NC	NC	9J
25	NC	NC	NC	9K
26	DQ1	DQ4	DQ13	10J
27	NC	NC	DQ4	11J
28		ZQ		11H
29	NC	NC	NC	10G
30	NC	NC	NC	9G
31	NC	DQ5	DQ5	11F
32	NC	NC	DQ14	11G
33	NC	NC	NC	9F
34	NC	NC	NC	10F
35	DQ2	DQ6	DQ6	11E
36	NC	NC	DQ15	10E

Bit	Się	gnal na	me	Bump		
no.	x8	x18	x36	ID		
37	NC	NC	NC	10D		
38	NC	NC	NC	9E		
39	NC	DQ7	DQ17	10C		
40	NC	NC	DQ16	11D		
41	NC	NC	NC	9C		
42	NC	NC	NC	9D		
43	DQ3	DQ8	DQ8	11B		
44	NC	NC	DQ7	11C		
45	NC	NC	NC	9B		
46	NC	NC	NC	10B		
47		CQ		11A		
48		_		Internal		
49		Α		9A		
50		Α		8B		
51	Α	A1	A1	7C		
52	NC	A0	A0	6C		
53		/LD		8A		
54	NC	NC	/BW1	7A		
55	/NW0	/BW0	/BW0	7B		
56		K		6B		
57		/K		6A		
58	NC	NC	/BW3	5B		
59	/NW1	/BW1	/BW2	5A		
60		R, /W		4A		
61		Α		5C		
62		Α		4B		
63	Α	Α	NC	3A		
64		/DLL		1H		
65		/CQ		1A		
66	NC	DQ9	DQ27	2B		
67	NC	NC	DQ18	3B		
68	NC	NC	NC	1C		
69	NC	NC	NC	1B		
70	NC	DQ10	3D			
71	NC	NC	DQ28	3C		
72	NC	NC	NC	1D		

Bit	S	ignal na	me	Bump
no.	x8	x18	x36	ID
73	NC	NC	NC	2C
74	DQ4	DQ11	DQ20	3E
75	NC	NC	DQ29	2D
76	NC	NC	NC	2E
77	NC	NC	NC	1E
78	NC	DQ12	DQ30	2F
79	NC	NC	DQ21	3F
80	NC	NC	NC	1G
81	NC	NC	NC	1F
82	DQ5	DQ13	DQ22	3G
83	NC	NC	DQ31	2G
84	NC	NC	NC	1J
85	NC	NC	NC	2J
86	NC	DQ14	DQ23	3K
87	NC	NC	DQ32	3J
88	NC	NC	NC	2K
89	NC	NC	NC	1K
90	DQ6	DQ15	DQ33	2L
91	NC	NC	DQ24	3L
92	NC	NC	NC	1M
93	NC	NC	NC	1L
94	NC	DQ16	DQ25	3N
95	NC	NC	DQ34	ЗМ
96	NC	NC	NC	1N
97	NC	NC	NC	2M
98	DQ7	DQ17	DQ26	3P
99	NC	NC	DQ35	2N
100	NC	NC	NC	2P
101	NC	NC	NC	1P
102		Α		3R
103		Α		4R
104		Α		4P
105		Α		5P
106		Α		5N
107		Α		5R



JTAG Instructions

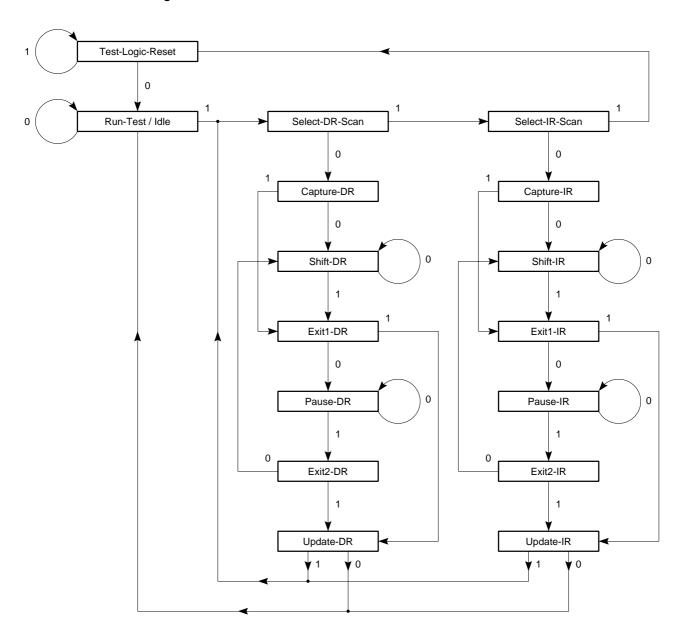
Instructions	Description
EXTEST	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-
	scan register cells at output pins are used to apply test vectors, while those at input pins capture test
	results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the
	boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST,
	the output driver is turned on and the PRELOAD data is driven onto the output pins.
IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in
	capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The
	IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed
	in the test-logic-reset state.
BYPASS	The BYPASS instruction is loaded in the instruction register when the bypass register is placed between
	TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the
	board level scan path to be shortened to facilitate testing of other devices in the scan path.
SAMPLE / PRELOAD	SAMPLE / PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE /
	PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture-DR
	state loads the data in the RAMs input and DQ pins into the boundary scan register. Because the RAM
	clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the
	I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing
	the TAP to sample metastable input will not harm the device, repeatable results cannot be expected.
	RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus
	hold time (tcs plus tch). The RAMs clock inputs need not be paused for any other TAP operation except
	capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state
	then places the boundary scan register between the TDI and TDO pins.
SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM DQ pins are forced to an
	inactive drive state (high impedance) and the boundary register is connected between TDI and TDO
	when the TAP controller is moved to the shift-DR state.

JTAG Instruction Coding

IR2	IR1	IR0	Instruction	Note
0	0	0	EXTEST	
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	1
0	1	1	RESERVED	
1	0	0	SAMPLE / PRELOAD	
1	0	1	RESERVED	
1	1	0	RESERVED	
1	1	1	BYPASS	

 $\textbf{Note 1.} \ \ \mathsf{TRISTATE} \ \ \mathsf{all} \ \ \mathsf{DQ} \ \mathsf{pins} \ \mathsf{and} \ \ \mathsf{CAPTURE} \ \mathsf{the} \ \mathsf{pad} \ \mathsf{values} \ \mathsf{into} \ \mathsf{a} \ \mathsf{SERIAL} \ \mathsf{SCAN} \ \mathsf{LATCH}.$

TAP Controller State Diagram



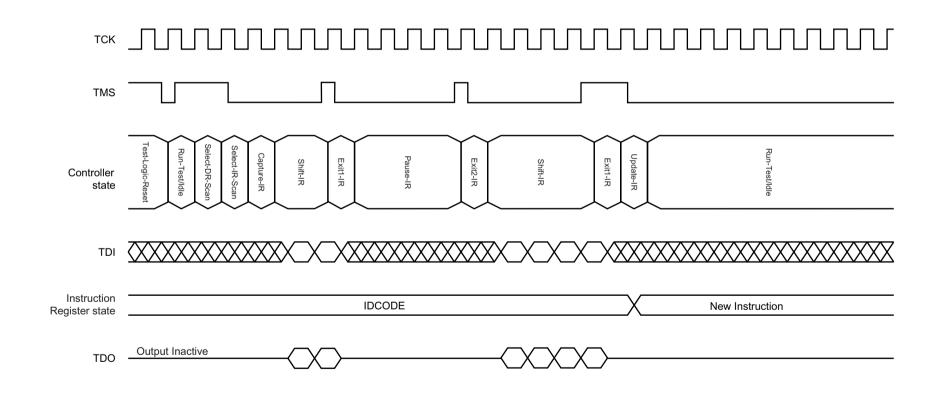
Disabling the Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to Vss to preclude mid level inputs.

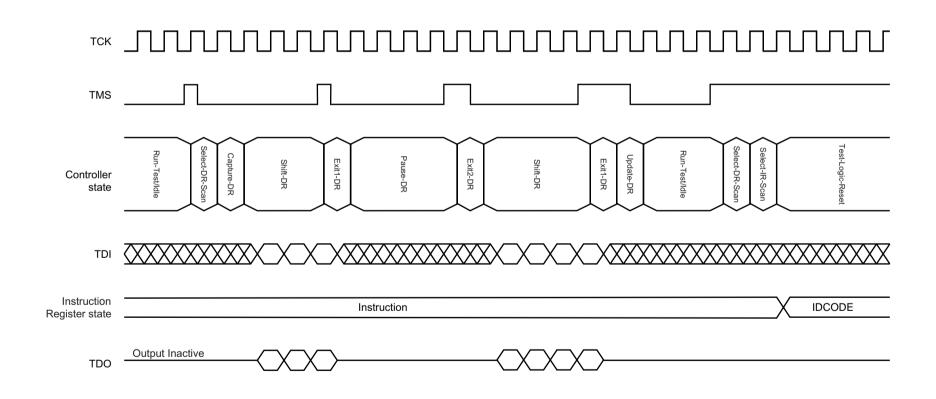
TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a 1 k Ω resistor.

TDO should be left unconnected.

Test Logic Operation (Instruction Scan)

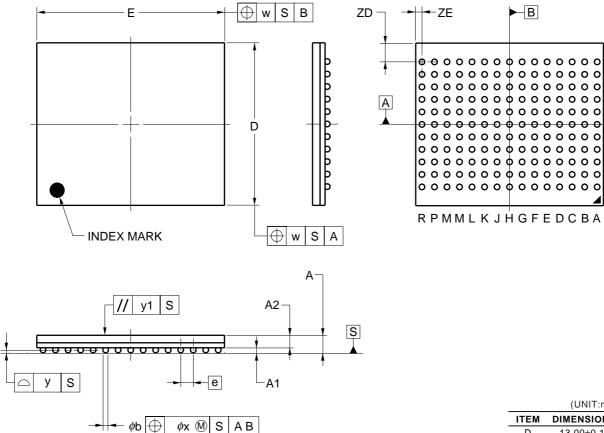


Test Logic (Data Scan)



★ Package Drawing

165-PIN PLASTIC BGA (13x15)



(UNIT:mm) DIMENSIONS D 13.00±0.10 Е 15.00±0.10 0.15 е 1.00 1.40±0.11 Α Α1 0.40±0.05 A2 1.00 0.50±0.05 b 0.08 Х 0.10 0.20 у1 ZD 1.50 0.50 ΖE P165F5-100-EQ1

Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of these products.

Types of Surface Mount Devices

μPD44164084F5-EQ1: 165-pin PLASTIC BGA (13 x 15) μPD44164184F5-EQ1: 165-pin PLASTIC BGA (13 x 15) μPD44164364F5-EQ1: 165-pin PLASTIC BGA (13 x 15)



Revision History

Edition/	Pa	ge	Type of	Location			Description						
Date	This	Previous	revision					(Previous edition $ o$ This edition)					
	edition	edition											
7th edition/	Throughout	Throughout	Deletion	Ordering Information				μPD44164364F5-E40-EQ1					
Feb. 2004	p.12	p.12	Modification	DC Characteristics IDD (MAX.)									
									_				
				MAX. Unit				MAX.		Unit			
						x8, x18	x36		╛.		x8, x18	x36	
					-E40	560	TBD	mA		-E40	620	-	mA
					-E50	480	530			-E50	540	620	
					-E60	410	480		_	-E60	470	570	
									•				
				DC Characteristics IsB1 (MAX.)									
						r			⊣		 		
					MAX. Unit				MA	X.	Unit		
						x8, x18	x36				x8, x18	x36	
					-E40	25	50	mA		-E40	320	-	mA
					-E50 210		-E50 210 -E50		27	270			
				-E60 190		_	-E60	250					
	p.26	p.26	Modification	Package Drawing				Preliminary version $ o$ Standardized version					

[MEMO]



[MEMO]

NOTES FOR CMOS DEVICES —

1 VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{\rm IL}$ (MAX) and $V_{\rm IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{\rm IL}$ (MAX) and $V_{\rm IH}$ (MIN).

(2) HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

4 STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

Data Sheet M15822EJ7V1DS 31

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